SMART LOCK SYSTEM

DESIGN

Our main object is to utilize the different electronic parts available in the market and build an integrated home security system based on ICs, microcontroller and wireless technology to give service at low cost compared to the cost of the conventional security system.

# Flow Chart Of Operation

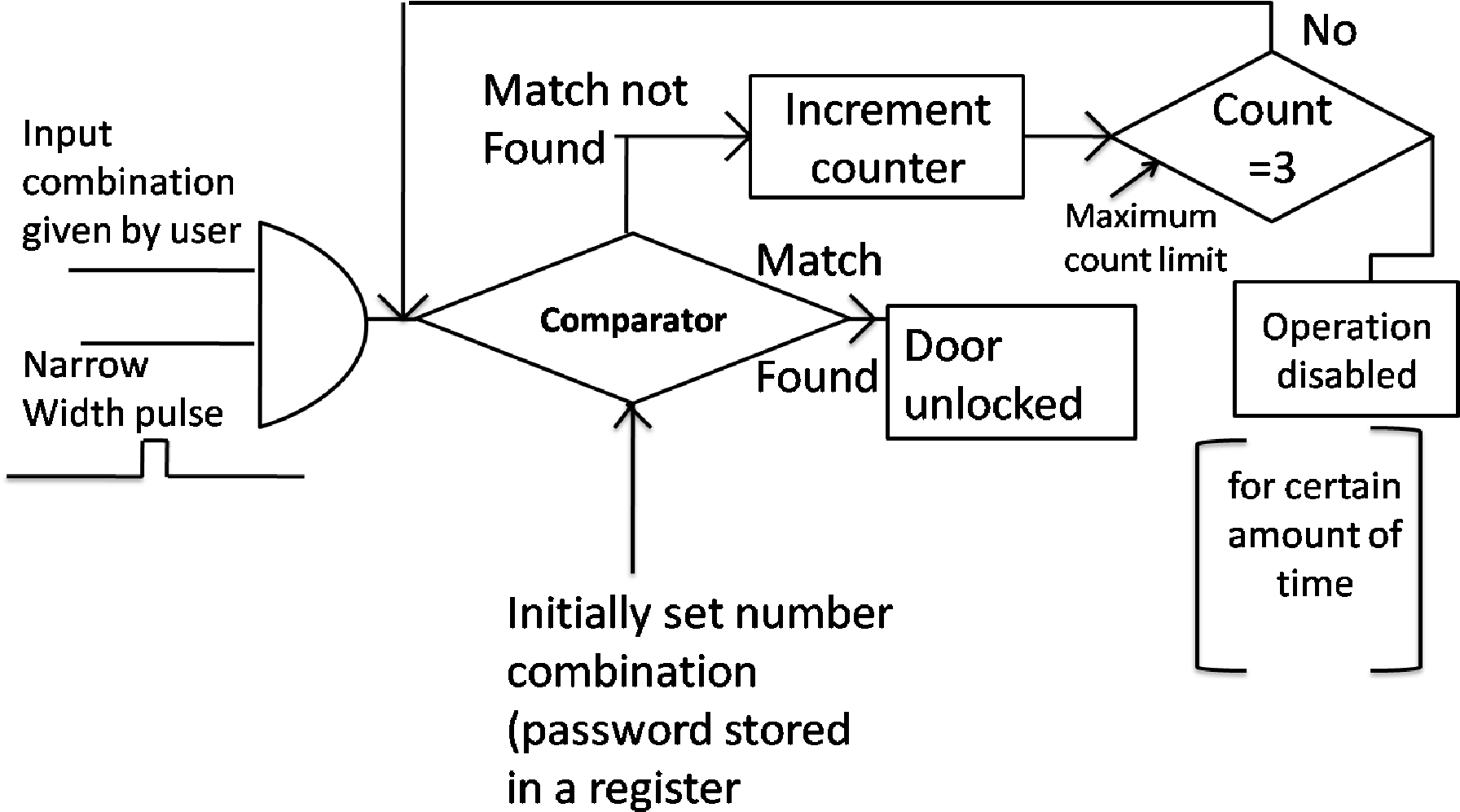


Fig. 1. Flowchart of the proposed project

In this figure the first block is the AND gate where we gives two inputs 1) input combination given the user 2) narrow width pulse. Mainly the input combination decides that the password (which is stored in a 8-bit shift register) is either matched or not. We should allow the input combination for a brief instant of time. So that the same input will be unable to trigger the counter circuit more than once thus preventing our circuit getting disable by one erroneous combination. So that we have to use narrow width pulses ANDed with input combination.

# Bit Shift Register (74164)

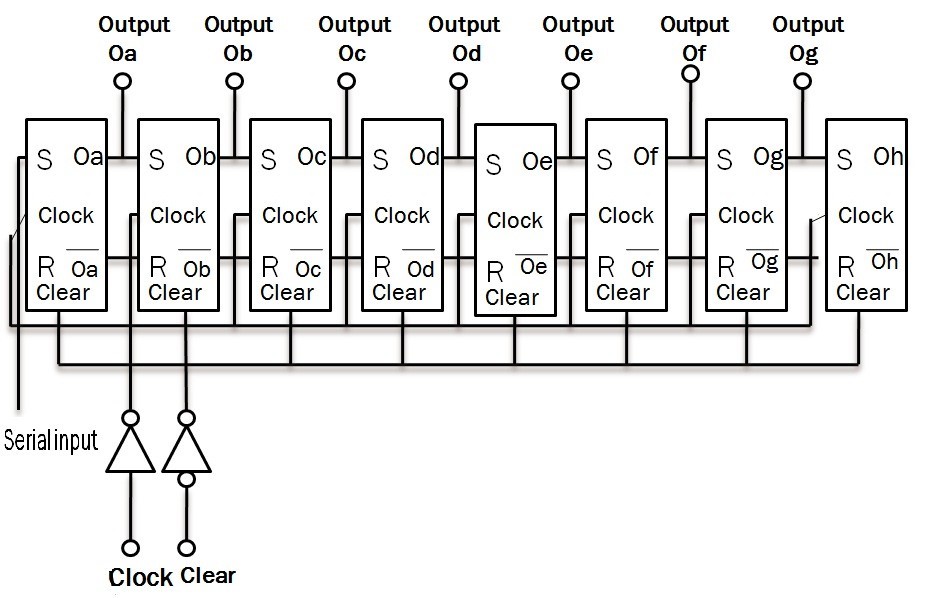


Fig. 2. 8 Bit Shift Register (74164)

# Digital Bitwise Magnitude Comparator Circuit

Comparison of two bit patterns (A7A6A5A4A3A2A1A0, B7B6B5B4B3B2B1B0) is obtained by using XNOR gates. Because when a two input XNOR gate receive two inputs both are equal, it produces 1 in its output, and 0 when two bits are unequal.

X Θ Y = XY + X’Y’

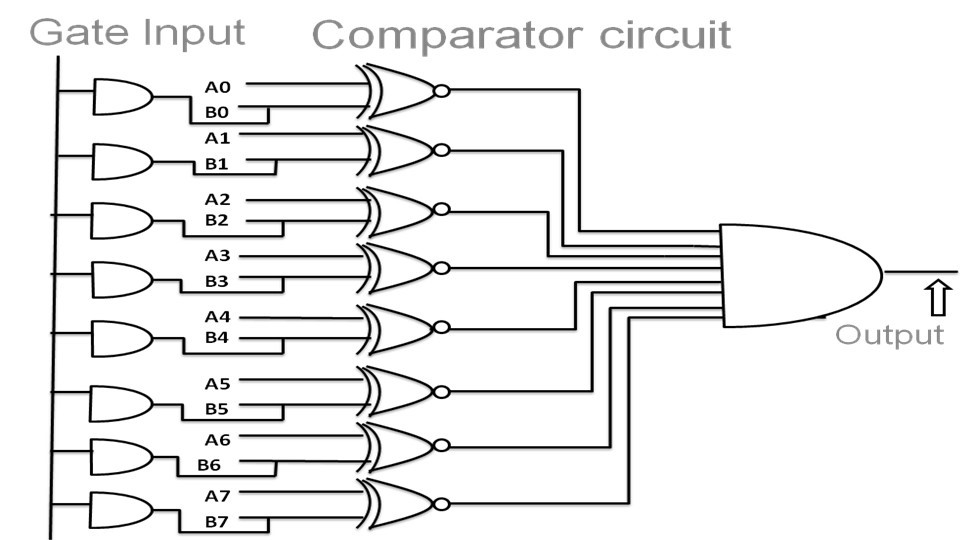


Fig 3. Digital Comparator Circuit

# Digital Synchronous Up Counter

In synchronous up counter, the term Q1, Q2,.. called carry i.e. it is brought forward to each stage. Carry must ripple through the successive and gates. It means that output of right most and gate will not valid until the output of all preceding and gate will not valid. The propagation delays of all and gates accumulated and this cumulative delay puts a limit on the counting speed of the synchronous up counter. Last flip flop will be changed for every clock pulse may be it is positive or negative edge according to what we are using. So, the last flip-flop j-k is permanently made 11. For the other flip flops are made conditionally made1-1. The condition of getting 1-1 is all its right hand side flip-flop is 1-1. When the output of the last flip- flop is ‘1’, it is applied to the next flip flop. Again depending on the clock pulse the output of the flip flop changes. The output of this flip flop and the previous flip flop is applied to the next. Only if the outputs are ‘1’ of the last two flip flops the output of the flip flop which is at the right side of the last two flip flops are changed and this process is continuous for all the respective flip flops.

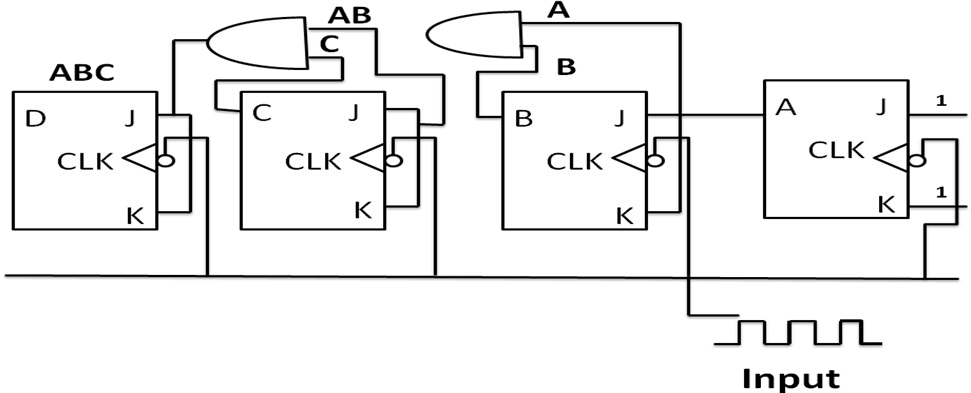


Fig. 4. synchronous up counter

# J-K Flip-Flop

We use JK flip-flop to design a counter which is a refinement of the RS flip-flop in that the indeterminate state of the RS type is defined in the JK type. Inputs J and K behave like inputs S and R to set and clear the flip-flop. When inputs are applied to both J and K simultaneously, the flip-flop switches to its complement state, that is, if Q=1, it switches Q=0, and vice versa.

A clocked JK flip-flop is shown the above Fig 5(a). Output Q is ANDed with K and CP inputs so that the flip-flop is cleared during a clock pulse only if Q was previously 1. Similarly, output Q is ANDed with J and CP inputs so that the flip-flop is set with a clock pulse only if Q was previously 1.

As shown in the characteristic table in Fig 5(c), the flip-flop behaves like an RS flip-flop, except when both J and K are equal to 1. When both J and K are 1, the clock pulse is transmitted through one AND gate only – the one whose input is connected to the flip-flop output which is presently equal to 1. Thus, if q=1, the output of the upper AND gate becomes 1 upon application of a clock pulse, and the flip-flop is cleared. If Q=1, the output of the lower AND gate becomes a 1 and the flip-flop is set. In either case, the output state of the flip-flop is complemented.

The inputs in the graphical symbol for the JK flip-flop must be marked with a J (under Q) and K (under Q).

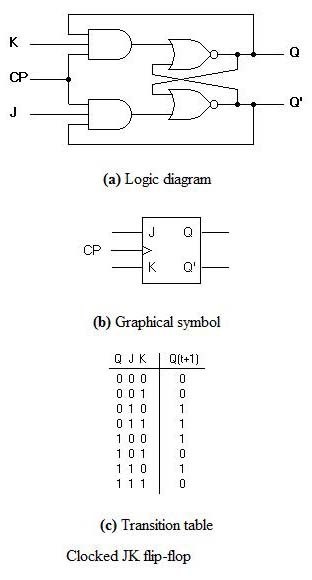


Fig. 5. J-K flip-flop

# Edge Triggering In Flip-Flops

We use edge triggering for the each flip-flops in the digital counter so that the counter will only be incremented in a short duration of time to avoid a single wrong combination to increase the count value more than once. A clock pulse goes through two signal transitions from 0 to 1 and returns from 1 to 0. As shown in Fig 6, a positive transition is defined as the positive edge and a negative transition as the negative edge. This definition applies also to the negative pulses. The term edge-triggered means that the flip-flop changes its state either at the positive edge (rising or leading edge) or at the negative edge (falling or trailing edge) of the clock pulse and are sensitive to its inputs only at this transition of the clock.

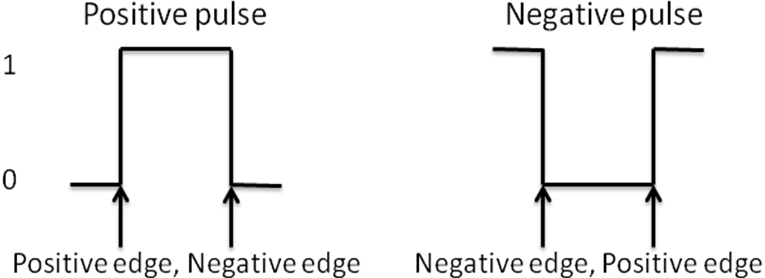


Fig 6. Definition of clock pulse transition

One way to make the flip-flop respond only to a pulse transition is to use capacitive coupling. An R-C (resistor- capacitor) circuit must be inserted in the clock input of the flip-flop. By deliberate design, the RC tine constant is much smaller than the clock’s pulse width. Because of this, the capacitor can charge fully when the clock goes high; this exponential charging produces a narrow positive voltage spike across the resistor

For your final project, you are to design an access control system based on a sequence of 6 bits that accepts a 1-bit at a time, either 0 or 1. This could be implemented with a 2-button keypad (o and 1), used to enter the binary code.

A second input functions as the *Enter* key, which ends the key code entry. As the key is entered, the device outputs Enter = 0 until the input sequence terminates. If the input sequence matches the After two unsuccessful attempts (i.e. the secret code was not matched), the system shuts down and won’t accept any more bits, and an alarm is triggered. Thus, your circuit has a second output Alarm, which is set to 1 after two unsuccessful attempts.

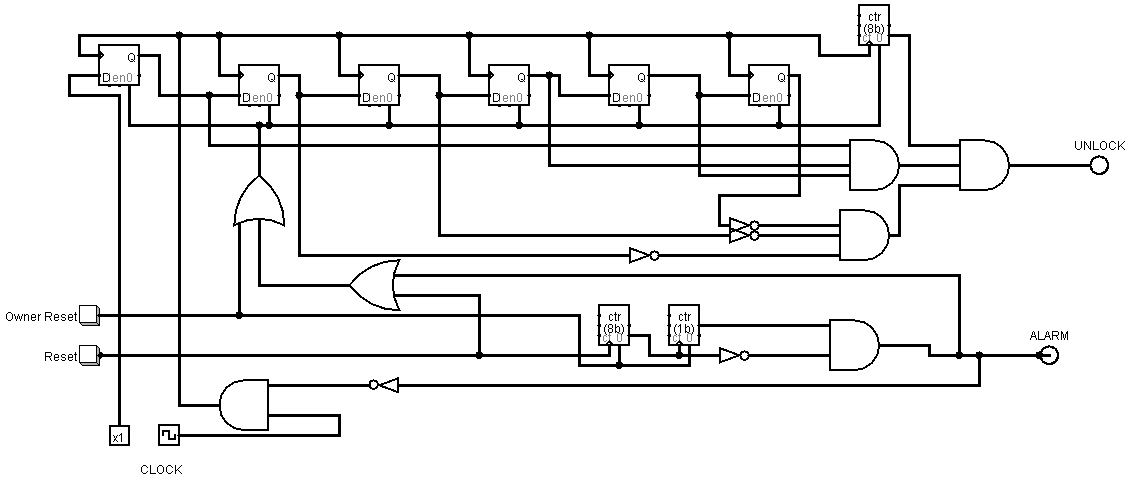
Extra credit: Add a reset to the system that presumably only the owner could control: when the reset key is inserted, the system is again enabled and can accept bits again. You can code the reset as either 0 (no key) or 1 (key inserted) for this project.

Secret code:

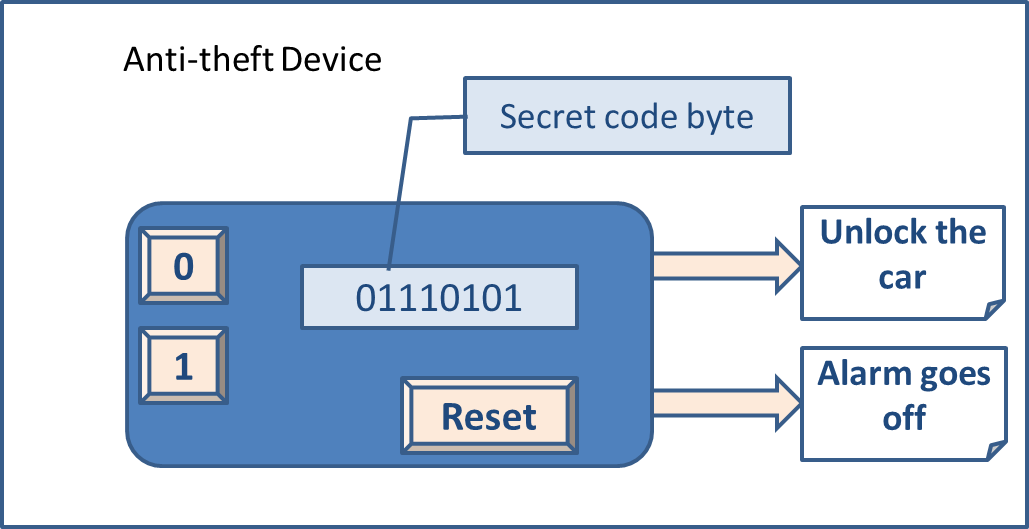
* Each of you has their very own secret code: no 2 people in the class can have the same code
* Your code can NOT be a simple sequence of all 1s or all 0s, and must contain a minimum of 2 ones and 2 zeroes

For this final project, you are allowed to work together on design, but each student’s solution will be unique, because each of you has a different secret code.

access code, then output Enter =1 (for example LED lights up), which will unlock the door in a full implementation. The secret code is preset: choose your own code (see below).



A schematic of the device is shown in the figure below for a secret code of 8 bits..



**Security Control Device**

DESIGN RESULT AND STATES

The timing interval is independent of the supply voltage. It may also be noted that once triggered, the output remains in the HIGH state until time elapses, which depends only upon R and C. Any additional trigger pulse coming during this time will not change the output state. However, if a negative going reset pulse is applied to the reset terminal during the timing cycle, transistor Q2 goes off,Q1 becomes on and the external timing capacitor C is immediately discharged. It may be seen that the output of Q2 is connected directly to the input of Q1 so as to turn on Q1 immediately and thereby avoid the propagation delay through the FF. Now, even if the reset is released ,the output will still remain LOW until a negative going trigger pulse is again applied at the terminal. Sometimes the monostable circuit mistriggers on positive pulse ,even with the control pin by pass capacitor.

